AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. – 10. (Canceled)

11. (New) A semiconductor device including:

a first conductivity type substrate comprised of a semiconductor having a band gap equal to or greater than 2.0 eV and having a low impurity concentration;

a first region formed in a first plane of the substrate and having the same first conductivity type as that of the substrate and having a resistance lower than that of the substrate;

a first electrode formed in another plane of the first region;

a second region formed in a second plane of the substrate and having said first conductivity type of that of the substrate; and

a second electrode formed on the second region, the semiconductor device comprising:

a trench formed in the second plane;

a control region formed from a bottom of the trench into the substrate and having a different conductivity type than that of the substrate; and

a control electrode formed on the control region,

wherein the second electrode is formed over the control electrode through an insulating film, and

wherein the control region having the different conductivity type than that of the substrate is formed on at least a part of sidewalls of the trench such that the control region is contacted with the second region.

12. (New) The semiconductor device according to claim 11,

wherein an insulating film is formed between the sidewall and the control region.

13. (New) The semiconductor device according to claim 11,

wherein a width of the control region is made narrower on the second region side than on the first region side.

14. (New) The semiconductor device according to claim 11,

wherein a plurality of trenches are provided, each having a corresponding control region, and

wherein channel regions are respectively formed between adjacent ones of the control regions.

15. (New) A semiconductor device according to claim 14,

wherein sidewall portions adjoining the sidewall adjacent ones of the control regions of the trenches are comprised of an MOS channels.

16. (New) The semiconductor device according to claim 11,

wherein the control region in contact with the sidewall of the trench is formed with a Schottky contact to provide a MESFET.

17. (New) The semiconductor device according to claim 11,

wherein the second electrode is formed over an entire surface of the unit device.

18. (New) A semiconductor device including:

an n-type drift region with a low impurity concentration and a band gap of 2.0 eV or higher;

an n-type drain region formed in a first plane of the drift region and having a lower resistance than the drift region;

a drain electrode formed in another plane of the drain region;

an n-type source region formed in a second plane of the region;

the semiconductor device comprising:

a trench formed in the second plane of the drift region;

a p-type gate region formed from a bottom of the trench into the drift region;

a gate electrode formed in the gate region,

wherein the source electrode is formed over the gate electrode through an insulating film, and

wherein the p-type gate region is formed on at least a part of sidewalls of the trench such that the p-type gate is contacted with the source drain.

19. (New) The semiconductor device according to claim 11,

wherein a plurality of trenches and a plurality of control regions are provided, and

wherein a narrowest portion of a channel region present under the second region and wedged between the control regions is located deeper than bottom portions of the trenches.

20. (New) The semiconductor device according to claim 17,

wherein a plurality of trenches and a plurality of gate regions are provided and

wherein a narrowest portion of a channel region present under the source region and wedged between the gate regions is located deeper than bottom portions of the trenches.

21. (New) The semiconductor device according to claim 11,

wherein said control region extends from the bottom of the trench to the second region to completely cover the sidewalls of the trench.

22. (New) The semiconductor device according to claim 18,

wherein said p-type gate region extends from the bottom of the trench to the second region to completely cover the sidewalls of the trench.

23. (New) The semiconductor device according to claim 14,

wherein the channel regions are narrower between areas of the control region adjacent the bottom of the trenches than between areas of the control regions adjacent to the second regions.

24. (New) The semiconductor device according to claim 22,

wherein the channel regions are narrowest at depth deeper than one half the junction depths formed between the second regions and the substrate.

25. (New) The semiconductor device according to claim 19,

wherein the narrowest part of the channel region is formed at a depth deeper than one half of a junction depth formed between the control region and the substrate.

26. (New) The semiconductor device according to claim 20,

wherein the narrowest portion of the channel region is formed at a depth deeper than one half of the junction depth formed between the gate regions and the substrate.